

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Bernd Deutschmann, et al. Art Unit : 2836
Serial No. : 10/588,984 Examiner : Dharti H. Patel
Filed : November 21, 2006 Conf. No. : 4272
Title : CIRCUIT ARRANGEMENT AND METHOD FOR PROTECTING AN
INTEGRATED SEMICONDUCTOR CIRCUIT

MAIL STOP RCE

Commissioner for Patents
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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

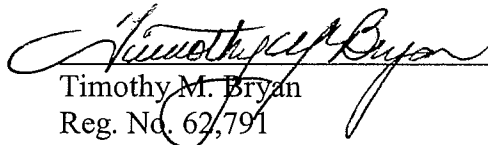
Please consider the references listed on the enclosed PTO-1449 form. Foreign patent documents and non-patent literature are enclosed; cited U.S. patents and patent application publications will be provided on request.

Submitted herewith are English abstracts for foreign language references 13 and 15. References 12 and 14 are also in a non-English language. Their respective corresponding English equivalents, i.e., reference 1 and 3, are provided.

This filing is being made with the filing of a Request for Continued Examination. No fee is required.

Respectfully submitted,

Date: January 20, 2010


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